REMARKS

The present application was filed on September 30, 2003 with claims 1-24. In response to a Restriction Requirement dated June 15, 2004, claims 13-24 were withdrawn from consideration. In the outstanding Office Action dated November 9, 2004, the Examiner has: (i) objected to the drawings under 37 C.F.R. 1.83(a); (ii) rejected claim 4 under 35 U.S.C. §112, first paragraph; (iii) rejected claims 1-12 under 35 U.S.C. §112, second paragraph; (iv) rejected claims 1-3, 5, 6, 10 and 11 under 35 U.S.C. §102(b) as being anticipated by Japanese Patent Publication No. JP 2001-15741 to Nakagawa Akio (hereinafter "Akio"); (v) rejected claims 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over Akio; and (vi) indicated that claims 9 and 12 are allowable.

In this response, the specification has been amended to correct an error of a typographical nature. Furthermore, claims 13-24 have been canceled without prejudice as being directed to a non-elected invention, claims 1, 9, 10 and 12 have been amended, and claims 25 and 26 have been added. Applicants traverse the §112, §102(b) and §103(a) rejections for at least the reasons set forth below. Applicants respectfully request reconsideration of the present application in view of the above amendments and the following remarks.

The Examiner has objected to the drawings for failing to show every feature of the invention specified in the claims (Office Action; page 3, paragraph 4). The Examiner contends that the feature "the buried LDD region being spaced laterally from the drain region," as recited in claims 1 and 10, must be shown or such feature must be canceled from the claims (Office Action; page 3, paragraph 4). In this regard, claims 1 and 10 have been amended in a manner which is believed to further clarify the correspondence between the claims and the drawings.

The Examiner contends that the drawings fail to show the feature "a first insulating layer under the gate and a second insulating layer under the shielding structure are formed of different thickness in comparison to one another recited in claim 4" (Office Action; page 3, paragraph 4). Applicants respectfully disagree with this contention. First, as set forth in 35 U.S.C. §113, a drawing need only be furnished "where necessary for the understanding of the subject matter sought to be patented." Applicants submit that the present specification provides a clear and unambiguous description for this additional feature of the claimed invention, and thus it is believed that such feature(s) need not be explicitly depicted in the drawing (see, e.g., page 11, lines 14-18 of the

present specification). Nevertheless, Applicants submit that the additional feature recited in claim 4 is shown generally in FIG. 4 as insulating layer 224. The specification states that the "various layers and/or regions shown in the accompanying figures may not be drawn to scale" (specification; page 4, lines 12-13; emphasis added), and that the insulating layer 224 beneath the gate 210 and dummy gate 230 may be referred to as gate oxide (specification; page 8, lines 19-20). Since the insulating layer 224 is not limited to any specific thickness, it is clear that FIG. 4 is intended to cover devices in which the gate oxide under the gate 210 and dummy gate 230 are of the same or different thicknesses relative to one another.

With regard to the objection to the drawings for failing to show a vertical diffused MOS device as recited in claim 7 (Office Action; page 3, paragraph 4), Applicants submit that such a feature is not essential for a proper understanding of the invention, but rather a vertical diffused MOS (DMOS) device is merely a specific type of MOS device, as is generically set forth in claim 1 and illustrated, for example, in FIG. 2. The present specification makes it clear that such vertical and lateral DMOS devices are within the scope of the claimed invention (see, e.g., specification; page 4, lines 3-7). Consequently, Applicants do not believe that such additional limitations of claim 7 need to be depicted in the drawings.

For at least the above reasons, Applicants assert that all elements recited in the claims that are necessary for a proper understanding of the invention are clearly depicted in the drawings. Accordingly, withdrawal of the objections to the drawings is respectfully solicited.

Claim 4 stands rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Examiner contends that the "specification and the drawings do not disclose a first insulating layer under the gate and a second insulating layer under the shielding structure are formed of **different thickness in comparison to one another** as recited in claim 4" (Office Action; page 5, paragraph 2; emphasis in original). Applicants respectfully disagree with this contention and assert that the present application provides ample support for such additional feature(s) set forth in claim 4. FIG. 2, for example, illustrates an insulating layer 224 in the general sense, which is intended to include the respective gate oxide layers under the gate and shielding structure (dummy gate). Furthermore, the specification clearly describes that the gate

oxide layers under the gate and dummy gate may be formed of different thicknesses. For instance, the specification, at page 11, lines 14-18, states:

> By forming the dummy gate 230 in a separate process step, the gate oxide 224 under the dummy gate, as well as other features of the dummy gate (e.g., shape), may be individually adjusted as desired. In a preferred embodiment of the invention, for example, the gate oxide 224 beneath the dummy gate 230 may be thinned by a predetermined amount, such as by using an etching process, compared to the gate oxide 224 under the gate 210. (emphasis added)

Since the features recited in claim 4 are clearly supported by the specification and drawings, Applicants respectfully request withdrawal of the §112 rejection of claim 4.

Claims 1-12 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner contends that, with regard to independent claims 1 and 10, it is unclear how the buried LDD region can be spaced laterally from the drain region, and how the second LDD region can be self-aligned with the gate and spaced laterally from the gate (Office Action; page 5, last paragraph to page 6, paragraph 2). Applicants respectfully disagree with this contention and submit that the shielding structure can, in fact, be self-aligned with the gate and yet still be spaced laterally from the gate, as explained in the present specification, for example, on page 10, lines 23-25. Nonetheless, independent claims 1 and 10 have been amended to further clarify the manner in which the second LDD region is self-aligned with the gate. Specifically, claims 1 and 10, as amended, recite (in part):

> . . . a second LDD region of the first conductivity type formed in the buried LDD region and proximate the upper surface of the semiconductor layer, the second LDD region being self-aligned with a first alignment structure formed substantially concurrently with the gate in a same processing step, the second LDD region being spaced laterally from the gate such that the gate is non-overlapping relative to the second LDD region.

As described in the present specification, the gate 210 and the alignment structure (e.g., dummy gate 230), being formed concurrently in the same processing step, are self-aligned with one another (specification; page 8, lines 17-19). Furthermore, the specification states that by using the dummy gate as a mask during the implant step to form the second LDD region, the second LDD

region will be self-aligned to the dummy gate, and will therefore be self-aligned to the gate (specification; page 13, lines 22-25).

For at least the reasons set forth above, Applicants believe that claims 1 and 10, as amended, are not indefinite. Accordingly, withdrawal of the §112 rejection of claims 1-12 is respectfully requested.

Claims 1-3, 5, 6, 10 and 11 stand rejected under 35 U.S.C. §102(b) as being anticipated by Akio. With regard to independent claims 1 and 10, the Examiner contends that Akio discloses all of the elements set forth in the subject claims. Applicants respectfully disagree with this contention. Claims 1 and 10, as amended, explicitly require that the second LDD region in the device be configured such that the second LDD region is "self-aligned with a first alignment structure formed substantially concurrently with the gate in a same processing step, the second LDD region being spaced laterally from the gate such that the gate is non-overlapping relative to the second LDD region." One benefit obtained from this configuration is that a device can be formed in which a distance between the second LDD region and the gate can be more accurately controlled, thereby ensuring that a proper electrical conduction path is formed between the buried LDD region and a channel region of the device (specification; page 13, lines 25-28). The prior art of record fails to teach or suggest a structure configured in the claimed manner. Rather, Akio, with reference to FIG. 1, discloses a device having a p-type reserve layer 19, which the Examiner analogizes with the second LDD region, formed at least partially below a gate electrode 33 (Akio; FIG. 1; English translated Abstract), and thus the gate overlaps the reserve layer.

Although Akio may disclose an embodiment in which the reserve layer 19 is formed in a non-overlapping relationship with respect to the gate electrode 33 (Akio; FIG. 11), Akio fails to disclose that the reserve layer is self-aligned with an alignment structure formed in the same processing step as the gate (and thus is also self-aligned with the gate), as explicitly required by claims 1 and 10. With reference to FIG. 11 of Akio, although Akio may disclose an electrode 45 formed on the upper surface of the device between the gate and the drain, the reserve layer 19 is formed below and extends completely beyond either end of the electrode. Consequently, the reserve layer 19 cannot be self-aligned with the electrode 45.

For at least the above reasons, Applicants submit that claims 1 and 10, as amended, are patentable over the prior art of record. Accordingly, favorable reconsideration and allowance of claims 1 and 10 are respectfully solicited.

With regard to claims 2, 3, 5 and 6, which depend from claim 1, and claim 11, which depends from claim 10, Applicants submit that these claims are also patentable at least by virtue of their dependency from their respective base claims. Moreover, one or more of these claims define additional patentable subject matter in their own right. Accordingly, favorable reconsideration and allowance of claims 2, 3, 5, 6 and 11 are respectfully requested.

Claims 7 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Akio. Specifically, the Examiner acknowledges that Akio "does not disclose the device is a vertical DMOS and the buried LDD [region] is formed in the semiconductor layer at a depth in a range from about 0.5 micron to about 2 micron and the second LDD region is formed in the semiconductor layer at a depth in a range from about 0.05 micron to about 0.5 micron" (Office Action; page 8, last paragraph), as required by the subject claims. However, the Examiner contends that "the type and depth differences are considered obvious design choices" which are not patentable unless unobvious or unexpected results are obtained (Office Action; page 8, last paragraph). While Applicants respectfully disagree with this contention, Applicants submit that claims 7 and 8, which depend from claim 1, are also patentable at least by virtue of their dependency from claim 1, which is believed to be patentable for at least the reasons set forth above. Accordingly, favorable reconsideration and allowance of claims 7 and 8 are respectfully solicited.

Claims 25 and 26 have been added. Applicants assert that claim 25, which depends from claim 1, and claim 26, which depends from claim 10, are also patentable over the prior art of record at least by virtue of their dependency from their respective base claims, which are believed to be patentable for at least the reasons set forth above. Moreover, these claims define additional patentable subject matter in their own right. For example, claim 25 further defines the device as being configured such that "the first alignment structure is removed after forming the second LDD region." Support for this additional feature can be found in the present specification, for example, on page 11, lines 18-22. The prior art of record fails to teach or suggest self-aligning the second LDD region with an alignment structure, and furthermore fails to teach or suggest removing the

alignment structure after forming the second LDD region, as required by the subject claims. Accordingly, favorable consideration and allowance of claims 25 and 26 are respectfully requested.

In view of the foregoing, Applicants believe that claims 1-12, 25 and 26, which are currently pending in the application, are in condition for allowance, and respectfully request withdrawal of the §112, §102 and §103 rejections.

Respectfully submitted,

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